7.6 A 128-Channel 6mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Tansmitter

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Simultaneous neural signal recording from many neurons has a wide range of applications ranging from the study of the complex biological neural networks to brain controlled neural prostheses to treat spinal cord injuries by restoring limb movement [1]. Wireless transmission of the recorded signals combined with on-chip neural spike sorting (a recording electrode senses the activity of an ensemble of neurons) is required for miniaturized and untethered neural recording systems. For neural prosthetic applications where the neural signals are translated to command signals for muscle stimulation, on-the-fly spike sorting and calibration is crucial for effective restoration of limb movement. Also, all these critical functions should be low power and wirelessly powered or operated on rechargeable battery.

Recently reported ICs for neural recording have features of simultaneous multiple channel recording [2,3], wireless data telemetry (spike information for 100 channels and raw data for one channel) [4], on-chip spike detection [4,5]. But a fully-integrated IC with simultaneous recording, on-chip spike detection *and* sorting and versatile wireless telemetry (raw and compressed data) has not been reported yet. This paper presents one such system with the capability to record, process and wirelessly transmit multiple neural signals real-time.

The chip is composed of eight 16-channel front-end blocks, data serializing circuits, a DSP for on-chip spike sorting, digital MUX, encoder, UWB TX, and bias generators (Fig. 7.6.1). The chip operates in one of the two modes. In sorting mode, a selected channel is connected to the on-the-fly spike sorting block and the extracted features of the spikes are transmitted for off-chip classification. In streaming mode, all the sampled data from the 128 channels are recorded and transmitted without any additional processing.

The front-end block consists of preamplifiers, buffers, an analog MUX, a second amplifier and a SAR-ADC (Fig. 7.6.2). The amplifiers are designed to have variable gain and bandwidth to meet the requirement of biological experiments. 16-to-1 multiplexing is chosen to minimize the power-area product of the entire system [6]. The preamplifier uses ac-coupling to reject the large dc offset occurring at the electrode-tissue interface [4]. The gain of the preamplifier is 40dB, and the second amplifier following the analog multiplexer provides an additional gain of 17dB to 20dB according to external controls. The high frequency roll-off of the preamplifier is variable from 2kHz to 20kHz in 16 steps by varying the load capacitance C_L. The low frequency roll-off is variable from 0.1Hz to 200Hz by changing the gate voltage V_B of the NMOS used as bias resistors. The gate voltage provided by the bias generator is variable from 600mV to 1V by 50mV steps. A fully-differential self-biased OTA enables a large 90dB CMRR and 80dB PSRR with $4.9\mu V_{rms}$ input-referred noise. Each preamplifier draws only 2μA and each buffer draws 20.3μA to drive the analog multiplexer. The amplifier after the multiplexer driving 10pF draws 40.6μA. A large reduction in power consumption is achieved by the *sequential turn-on* method in front-end blocks by 71% (7.5mW). Due to the time-multiplexing architecture of the system, not all the channels have to be turned on. Therefore, only two of the 16 channels are turned on at any one time. For example, only the first and second channels are turned on when a sample from the first channel is digitized (Fig. 7.6.2). A SAR-ADC is used for sampling and digitizing multiplexed signals at 40kSample/s/channel resulting in 640kSample/s. The resolution of the ADC can be adjusted from 6 to 9 bits. The reference voltage for the ADC is supplied by the bias generators and variable from 100mV to 500mV by 50mV steps.

Traditional spike feature extraction algorithms, such as principal component analysis (PCA), require frequent training through thousands of spike sequences [7]. Thus more than 1Mb/channel memory is required, which precludes a small area and low power implementation. Previous on-chip spike detections [3-5] use thresholding circuitry that would result in information loss of the features of the neural signals. Figure 7.6.3 shows the algorithm that enables the on-chip spike feature extraction. A noise shaping filter is used to reduce the neuronal noise as well as manifest neurons' geometry signatures. This filter combined with a max-min detector extracts the features, and enables the subsequent classification schemes to produce more precise clusters than PCA.

Figure 7.6.4 shows the on-chip on-the-fly spike detection and feature extraction engine. The 9 bit serial ADC output containing the time-multiplexed neural signals is fed to the spike detection and sorting units. The serial output data after the sorting consists of spike features in the form of three 9 bit scores per action potential. The data is processed, encoded and fed to the UWB TX on-the-fly within 41 cycles (1.025ms). The clustering of the scores received at the UWB RX is done off-chip. The coefficients register array is pre-loaded with 32 values, 9 bits each, which are computed within a few seconds of the initial recordings.

The 3.1 to 10.6GHz spectrum assigned by the FCC for unlicensed use of ultra-wideband devices offers an opportunity for short range, high data rate wireless communication. Impulse radio type UWB uses short pulses for transmission and this makes the TX design very simple, small-area, and low-power while providing data bandwidths of up to 90Mb/s for the simultaneous recording of more than 100 channels. These features make the impulse radio UWB one of the best candidates for the wireless telemetry for multi-channel neural recording systems [8]. The sampled and serialized data is Manchester encoded and then OOK or PPM modulated. Redundant data is inserted between every sampled data packet to be distinguished at the receiver side. Short pulses are generated according to the modulated signal, passed through a BPF for the transmitted signal to fit under the FCC emission mask and fed into the off-chip UWB antenna. The UWB RX was built from off-the-shelf components since it is outside the biological systems. The received signal is passed through a BPF whose center frequency is 4GHz, and then amplified by the LNA stages. A diode and a LPF down converts the UWB signal to low-frequency and the baseband data is finally recovered by an FGPA (Fig. 7.6.5).

The IC was fabricated in a 0.35μm 4M2P CMOS process and the chip size is $8.8\times7.2mm^2$ (Fig. 7.6.6). The measured power consumption of the entire chip is 6mW from ±1.65V when operating in streaming mode. The 8 front-end blocks consume 50% of the total power. The UWB TX consumes 1.6mW with PPM modulation. The power consumption of the DSP block is only 0.1mW. The chip was first tested with signal generators to evaluate the performance of each circuit block and measurement results are summarized in Fig. 7.6.7. Extracelluar recordings were made from a dissected snail brain to verify the functionality of the entire system. Waveforms at the output of amplifier, spike sorting, UWB TX, UWB RX were monitored by the built-in test circuits (Fig. 7.6.7).

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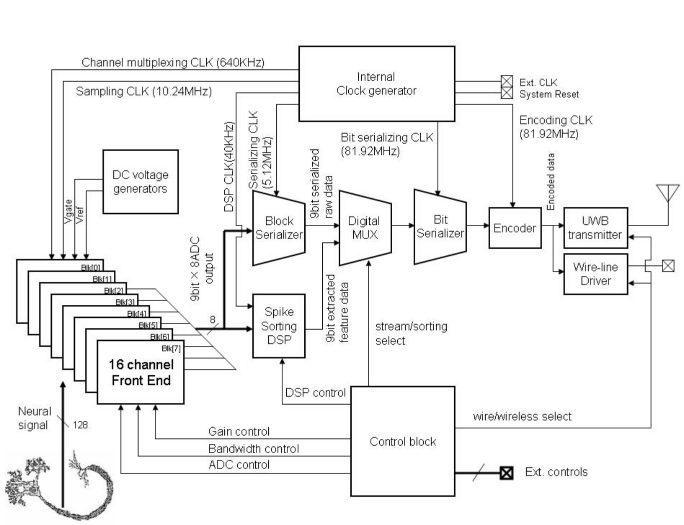


Figure 7.6.1: Block diagram of the integrated neural recording system.

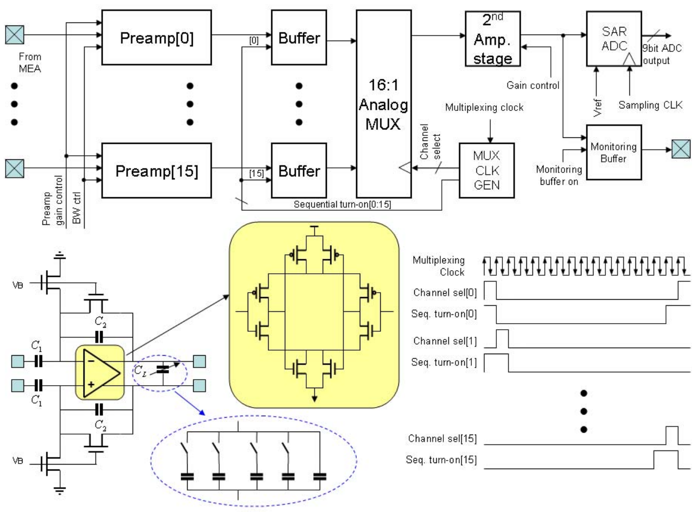


Figure 7.6.2: Schematic of 16-channel front-end blocks (Sequential turn-on scheme is used to reduce the power consumption).

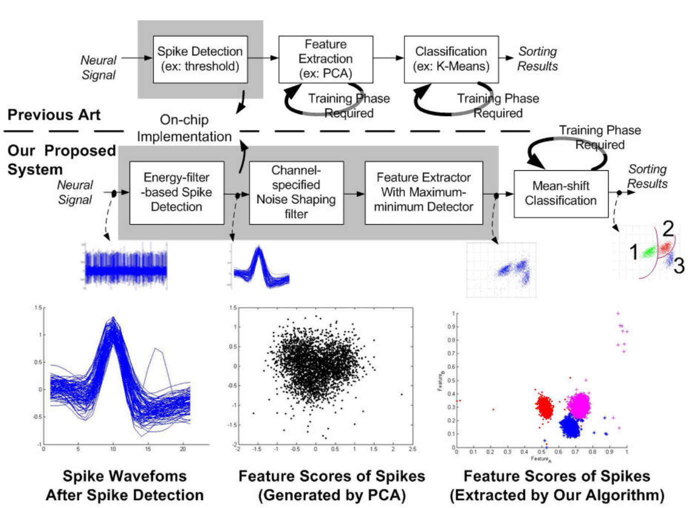


Figure 7.6.3: Proposed spike sorting algorithm.

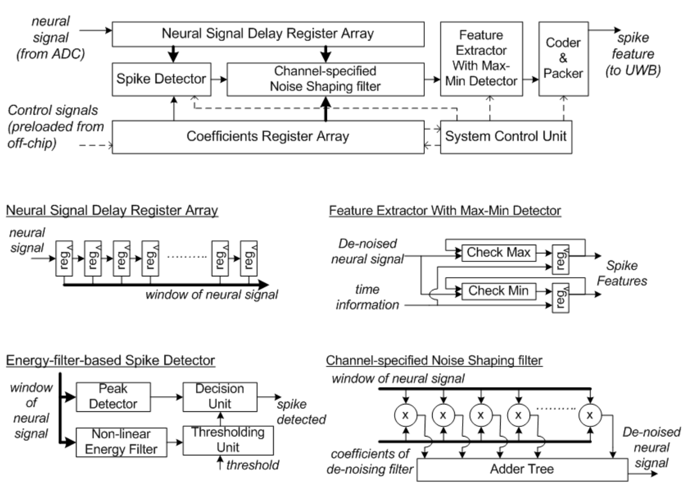


Figure 7.6.4: Block diagram of an on-line spike sorting engine.

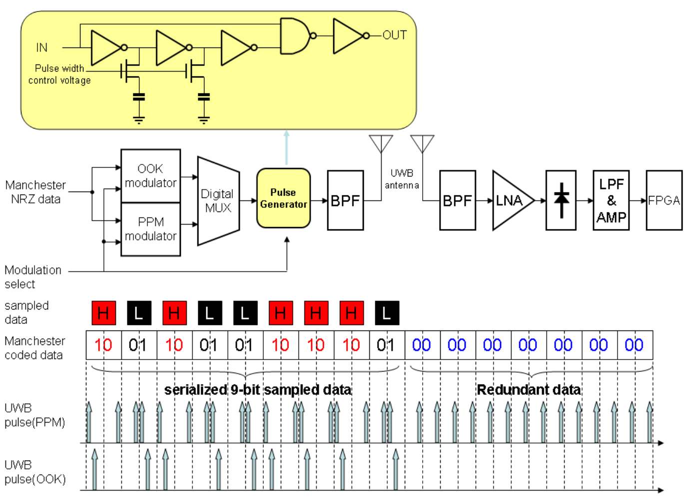
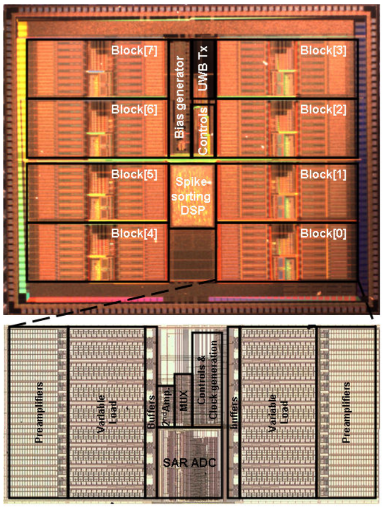


Figure 7.6.5: Block diagram of UWB transmitter and receiver.



Measured performance	
Number of channels	128
Signal gain of the preamp	40dB
Input impedance (at 1KHz)	8MΩ
Input referred noise	4.9μV_{rms}
CMRR of the preamp	90dB
PSRR of the preamp	80dB
LF roll-off of the preamp	0.1Hz ~ 200Hz *
HF roll-off of the preamp	2KHz ~ 20KHz *
Signal gain of the 2nd amp	17dB ~ 20dB *
ADC resolution	6 ~ 9 bits *
ADC sampling rate	640Ksample/sec
Power dissipated by DSP	0.1mW
Maximum UWB data rate	90Mbps
Power dissipated by UWB	1.6mW
Power supply level	±1.65V
Total chip power dissipation	6.0mW
Technology	0.35μm 4M2P CMOS
Total chip area	8.8mm ×7.2mm

* specification is programmable through external controls

Figure 7.6.6: Chip micrograph and performance summary.

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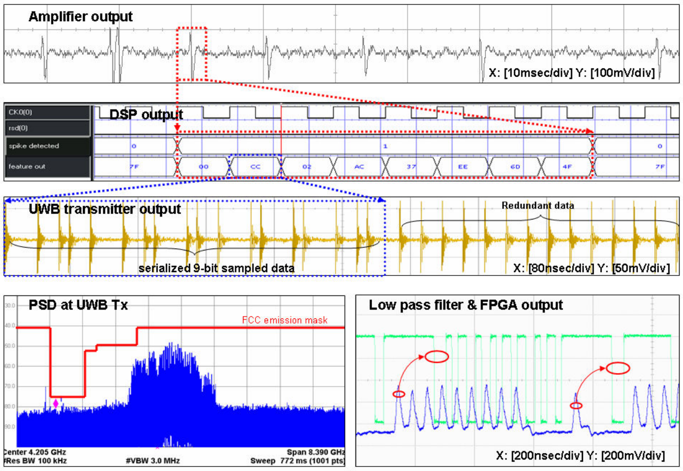

Figure 7.6.7: Measurement results of the IC with neural signal from a snail brain.